

Challenges in Semiconductor Front-End Processing, Modeling, and Simulation

Martin D. Giles

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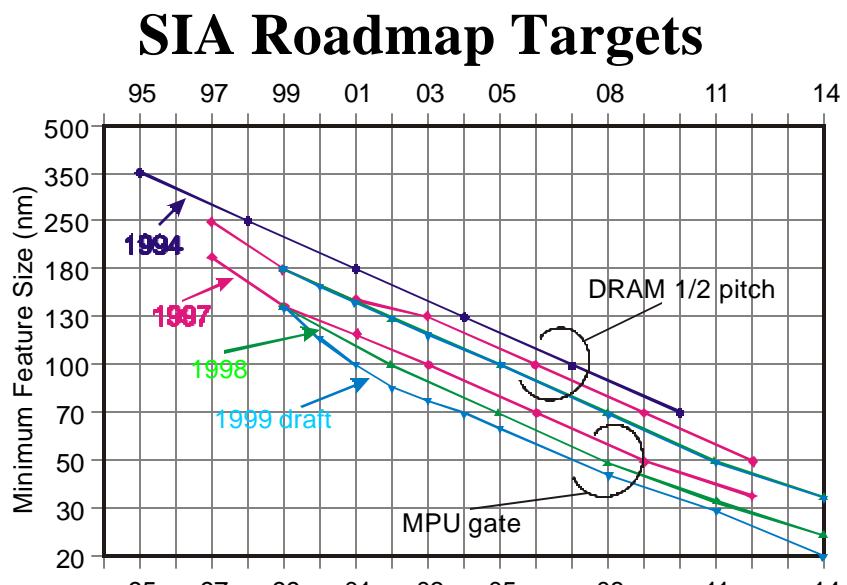
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Roadmap “Difficult Challenges”

Selected challenges for Front-end Process and Modeling:

- ◆ Before 2005, $\geq 100\text{nm}$
 - Nitride derivatives and High-K for gate stacks
 - Ultra-shallow junction formation methods and models
 - Metrology
- ◆ Beyond 2005, $< 100\text{nm}$
 - Ultra High-K materials and models for gate stacks
 - Alternate and ultra-scaled transistor structures and models
 - Integration of silicon compatible materials
 - Atomistic process modeling
 - Metrology



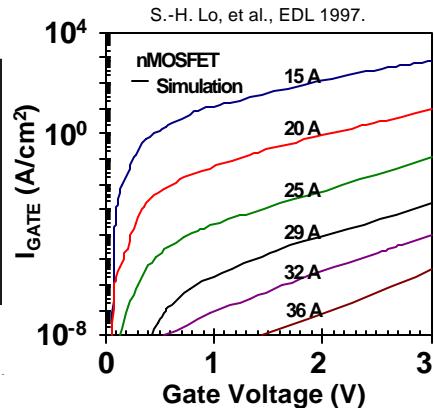
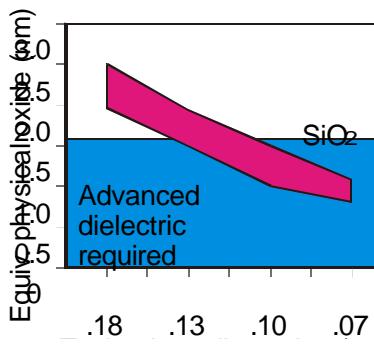
Outline

- ◆ Introduction
- ◆ Gate Stack challenges
- ◆ Source/drain doping challenges
 - Effect of junction scaling on devices
 - Physics of dopant diffusion and activation
 - Directions for research
- ◆ Other front-end challenges
- ◆ Conclusions

Gate stack: summary of issues

- ◆ Achieving required effective oxide thicknesses:
~1.2nm for nitride, <1.2nm for High-K by 2005
- ◆ Achieving optimal channel mobility >95% of SiO₂
- ◆ Minimizing gate leakage to achieve <1A/cm²
- ◆ Control Boron penetration
- ◆ Minimize gate electrode depletion
- ◆ Develop metal gates with appropriate workfunctions
- ◆ Thermal budget compatible with doping needs

Scaling Limit for SiO₂



$$I_{GATE} @ V_{CC}=1V \sim 1\text{A}/\text{cm}^2 \Rightarrow T_{OX}^P \text{ limit } \sim 1.6\text{nm} \text{ (EOT 2.3nm)}$$

Scott Thompson et.al., Intel Technology Journal, Q3 1998



Alternatives to SiO₂

- ◆ Silicon nitride / Nitrided oxide
 - Improves resistance to boron penetration
 - Not a large improvement in minimum EOT (lower tunneling barrier)
 - Potentially useful as thin barrier layer in stacked dielectrics
- ◆ Medium-K dielectrics (10-20)
 - Candidate materials Ta₂O₅, TiO₂, ZrO₂, ...
 - Currently being investigated by several universities
 - Results reported for EOT down to ~1.0nm
 - Promising, but many issues still be be resolved before viable
- ◆ High-K dielectrics (50+)
 - Suitability for gate dielectric not yet clear



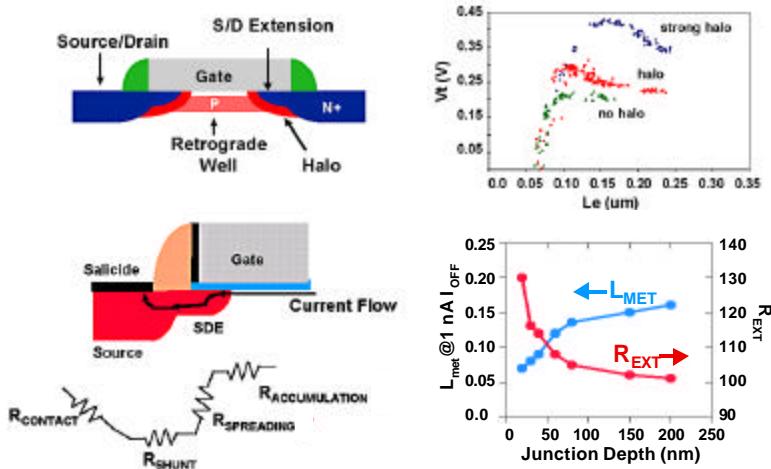
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Doping: summary of issues

- ◆ Controlling vertical and lateral diffusion
- ◆ Achieving low series resistance (<10% of channel R_s)
- ◆ Thermal budget compatible with gate stack needs
- ◆ Understanding dopant-defect interactions
- ◆ Interface effects on point defects and dopant
- ◆ Activation models and metastable states
- ◆ Amorphization/regrowth and extended defect generation
- ◆ Atomistic diffusion modeling

S/D and channel engineering requires understanding of diffusion and activation



Figures from "MOS Scaling: Transistor Challenges for the 21st Century",
Scott Thompson et.al., Intel Technology Journal, Q3 1998

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Doping by ion implantation

The diagram is divided into two panels:

- During implantation:** Shows an implanted ion (red sphere) hitting a silicon lattice. Blue spheres represent silicon atoms, and green spheres represent interstitial atoms. Arrows indicate the movement of atoms during the implantation process.
- Initial Stages of Annealing:** Shows the same implanted ion after implantation. It illustrates several processes:
 - Surface Recombination:** A blue atom moves from the surface back into the lattice.
 - Clustering:** Green atoms form small clusters.
 - Bulk Recombination:** A green atom moves from the surface into the bulk lattice.
 - “+1” Generation:** A new red ion is shown being generated.
 - Diffusion:** A blue atom moves away from its original position.

- Implanted Ion
- During implantation
- Initial Stages of Annealing
- Surface Recombination
- Clustering
- Bulk Recombination
- “+1” Generation
- Diffusion

◆ Implantation generates damage in the silicon lattice
◆ Silicon interstitials drive clustering and transient-enhanced diffusion

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Damage from 1keV Boron implant

A legend on the left identifies the symbols used in the diagram:

- Single Vacancies (yellow)
- Vacancy clusters (green)
- Single Interstitials (blue)
- Interstitial clusters (cyan)
- Boron active (red)
- Boron clusters (purple)

The diagram shows a 3D cross-section of a silicon wafer after a 1 keV Boron implant. The implant parameters are specified as 10^{14} ions/cm². The diagram includes dimensions: 150 nm width, 300 nm depth, and 50 nm thickness. Labels indicate the presence of Vacancies (green), Interstitials (blue), and Boron (red/purple) in various states (active or clusters).

After implantation of 1 keV B, 10^{14} ions/cm²

150 nm

300 nm

50nm

Boron

Vacancies

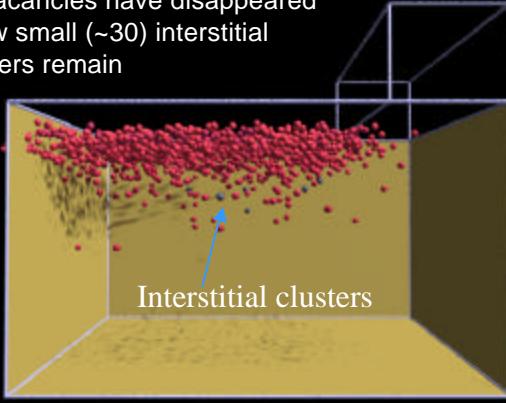
Interstitials

M. Caturla et.al. Lawrence Livermore National Laboratory

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Defect distribution after spike annealing

After 8s at 1050C
 - all vacancies have disappeared
 - a few small (~30) interstitial clusters remain



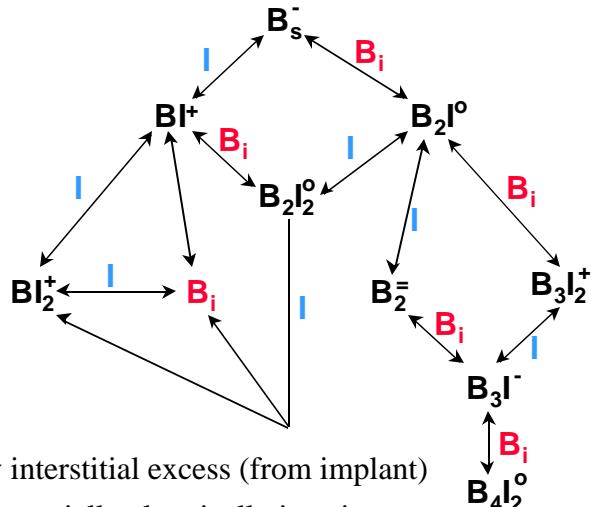
M. Caturla et.al. Lawrence Livermore National Laboratory

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Boron-interstitial clustering



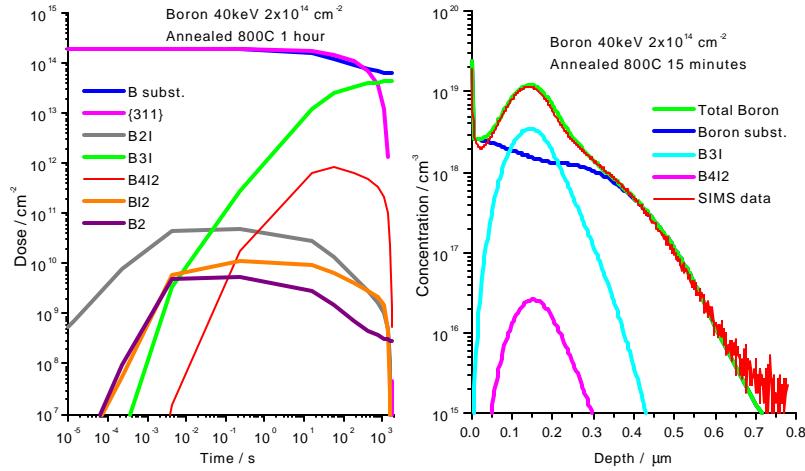
- ◆ Driven by interstitial excess (from implant)
- ◆ Immobile, partially electrically inactive

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Boron clustering during TED



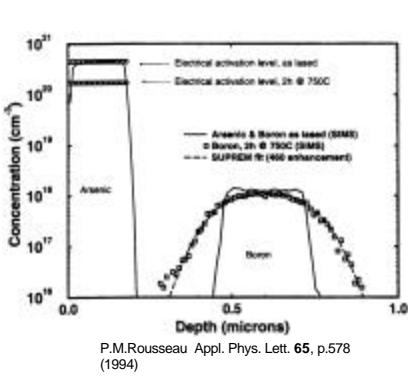
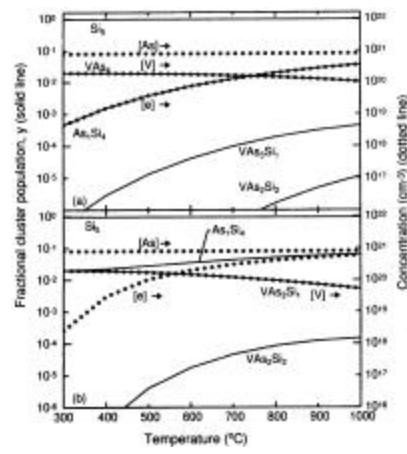
- ◆ Clustering driven by high interstitial concentrations
- ◆ Dissolution is very slow when TED is over

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Arsenic cluster deactivation

P.M.Rousseau Appl. Phys. Lett. **65**, p.578 (1994)M.A.Berding Appl. Phys. Lett. **72**, p.1492 (1998)

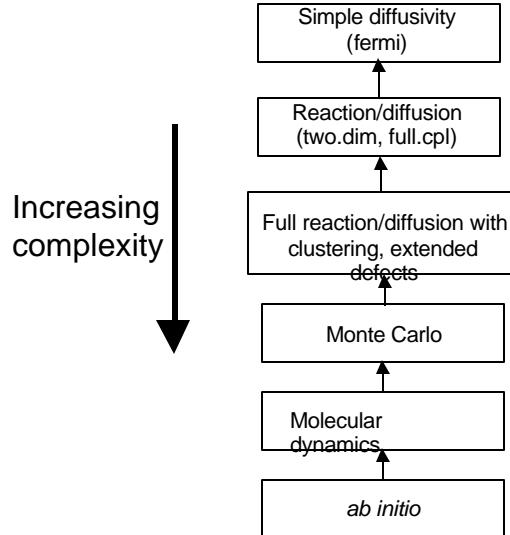
- ◆ $\text{As}_2\text{V} \Rightarrow \text{As}_3\text{V} \Rightarrow \text{As}_4\text{V}$
- ◆ Driven by high arsenic concentrations
- ◆ Even partial clusters can reduce electrical activation

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Diffusion modeling hierarchy



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Directions for research

- ◆ Understanding of dopant-defect behavior
 - Atomistic models for high doping, high temperatures
 - Amorphization/regrowth and extended defect kinetics
 - Details of activation/deactivation kinetics
- ◆ Approaches to improve activation
 - Metastable states (SPE, spike annealing, laser annealing, ...)
 - Extended systems (stress, codoping, ...)
- ◆ Alternatives that avoid implantation
 - Outdiffusion, epitaxy, Schottky contacts, ...

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Outline

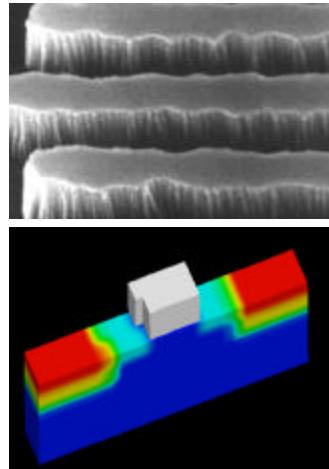
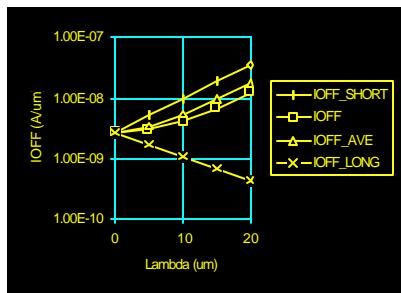
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Other front-end challenges: summary of issues

- ◆ Metrology
 - Need physical, electrical, and chemical measurement of
 - Gate dielectric stacks
 - Doping profiles in shallow junctions (vertical and lateral)
 - Gate electrodes and s/d contact schemes
- ◆ Control of device variation
 - Gate etch CD control and roughness
 - Atomic level fluctuations and statistical process variations

Example: Line Edge Roughness



- ◆ Line Edge Roughness effects both I_{ON} and I_{OFF} characteristics
- ◆ Small changes in local gate length strongly effect I_{OFF} while I_{ON} is much less sensitive

T.Linton et.al., 1999 VLSI Symposium

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Conclusions

- ◆ Delivering to the roadmap goals will require significant innovation in front-end materials, processes, and models
- ◆ Industry and university research programs (SRC, SEMATECH, ...) have made substantial progress in identifying potential directions, but much work remains
- ◆ Modeling and simulation will play a key role in understanding and guiding searches for solutions
- ◆ Implementing the solutions will bring new challenges in manufacturing and reliability as we add new materials and processes faster than ever before

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